Optimization and Comparison of Continuous and Discontinuous Current Source Drivers for MHz Boost PFC Converters*

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***Abstract* -- Comprehensive comparison of continuous and discontinuous Current Source Drivers (CSDs) are presented in terms of switching loss reduction and optimal design for MHz boost PFC converters. The advantages and disadvantages of the continuous and discontinuous CSDs are summarized based on the analysis and experimental results. Both of two drivers are able to achieve the functionality of the PFC boost converters. Overall, the discontinuous CSD achieve high efficiency over the continuous CSD owing to higher gate drive current. A 380V/200W output and 1-MHz boost PFC converter was built to verify the difference between these two types of the CSDs.**

***Index Terms*—Current Source Driver (CSD), power MOSFET, Boost converter, Power Factor Correction (PFC), Adaptive drive current.**

I. INTRODUCTION

With the development of the information technologies, the distributed power system (DPS) requires higher power density in the future. MHz switching frequency PFC applications are proposed to increase the power density of the DPS. However, MHz switching frequency results in high switching loss and gate drive loss [1]-[2], Recently, Current Source Drivers (CSDs) have been proposed to reduce the switching losses and gate drive loss in MHz switching frequency Voltage Regulators (VRs) applications. The idea of the CSD circuits is to build current sources to charge and discharge the power MOSFET gate capacitance so that the fast switching speed and the reduced switching loss can be achieved [3]-[7].

The dual channel low side CSD with one Current Source (CS) inductor was proposed for the interleaving boost converters in [8]. A dual channel high side and low side CSD using bootstrap technique was proposed to achieve the switching loss reduction and SR gate energy recovery in a buck converter in [9]. Based on an accurate analytical loss model, a general optimal method was proposed in [10] to find the trade off point of the switching losses and gate drive losses. A non-isolated resonant gate driver was proposed for the interleaving boost converters in [11].

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In order to reduce the CS inductor value, the CSD with discontinuous current was proposed in [12]-[13]. The key to this type of CSDs is to control of the driver switches to generate discontinuous inductor current waveforms enabling the peak portion of the current to be used to charge/discharge the power MOSFET as a nearly constant current source. In the above mentioned CSDs, the inductance value is typically 20nH at 1MHz switching frequency.

Most of previous work done with the CSDs is to investigate their applications in DC-DC converters, where the duty cycle normally has a steady state value. Presently, the full bridge (FB) CSD with the continuous inductor current achieving adaptive gate drive current was proposed for MHz PFC applications in [14]. The proposed solution can actually achieve adaptive drive currents inherently depending on the drain currents in the main power MOSFET to achieve optimal design. The similar idea has been also verified for the boost converter and synchronous buck converter with 1-MHz switching frequency to achieve high efficiency in wide load current range in [15]-[16]. In order to further reduce high frequency switching loss of MHz PFC boost converter with different load currents, the discontinuous CSD achieving adaptive gate drive current was proposed for MHz PFC applications in [17].

Considering the current waveforms of the CS inductors, the CSDs have two basic types: the continuous and the discontinuous. In this paper, comprehensive comparison between the continuous and discontinuous CSDs is presented in terms of the disadvantages and advantages. The optimal design is also given in the paper. The relationship between these two type of CSDs are also revealed, which provides deep insights of the CSDs in MHz PFC application.

II. CIRCUIT DESCRIPTIONS OF CONTINUOUS AND DISCONTINUOUS CSDS FOR PFC APPLICATIONS

In order to compare the properties of continuous and discontinuous CSD for MHz boost PFC converter, two types of the CSDs are introduced here. Fig. 1 shows the full-bridge (FB) CSD topology, which consists of four drive switches S_1-S_4. In Fig. 1, V_c is the drive voltage, L_r is the current source inductor. It is interesting to notice that this FB CSD is able to function in either CCM operation or DCM operation depending on the control scheme of the drive switches

1) CCM Operation

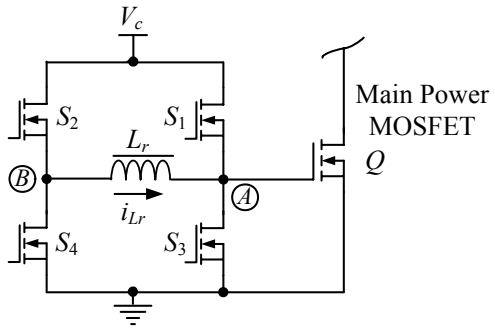


Fig. 1 CSD FB topology

Fig. 2 gives the key waveforms. The inductor current is continuous and triangle. The peak portion of the inductor current is used to turn on and turn off the main power MOSFET Q during $[t_0, t_1]$ and $[t_2, t_3]$ as shown in Fig. 2 respectively.

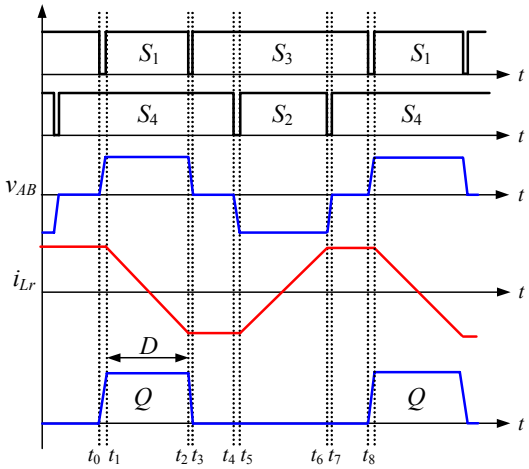


Fig. 2 Key waveforms of the continuous CSD

As seen from Fig. 2, S_1&S_3 and S_2&S_4 are complementarily controlled, which is similar to the control of the synchronous buck converters. Therefore, anther advantage of this solution is that the commercial off shelf components can be directly used instead of using discrete ones in other CSD circuits.

According to the voltage applied to the CS inductor, the peak inductor current I_{Lr_pk} is:

$$I_{Lr\_pk} = \frac{V_c \cdot D}{2 \cdot L_r \cdot f_s} \tag{1}$$

$$I_{Lr\_pk} = \frac{V_c \cdot (1-D)}{2 \cdot L_r \cdot f_s} \tag{2}$$

Fig. 3 shows the peak current value of the CS inductor, which is used to drive the main power MOSFET. It is observed that the drive current changes with the duty cycle and the value can be chosen when the CS inductor value is decided. As shown in Fig. 3, when the input line voltage below certain value, the CS inductor current changes adaptively with the boost inductor current. This means the drive current is able to behaviour adaptively according to the MOSFET switching current. Higher switching currents lead to higher CS drive currents, so this will drive the MOSFET faster and achieve lower switching loss.

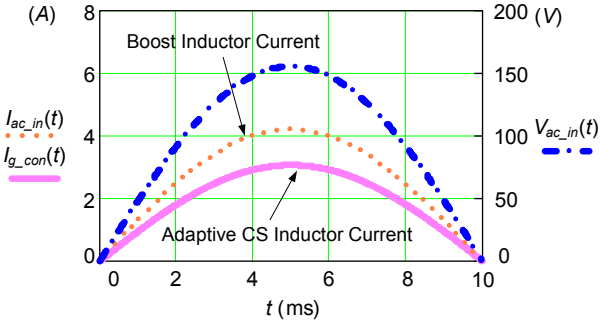


Fig. 3 Key waveforms of the continuous CSD

2) DCM Operation

The key waveforms are illustrated in Fig. 4. The inductor current i_{Lr} is discontinuous to minimize conduction loss compared to the continuous circulating current, where t_{10} is the pre-charge time and t_{21} is the turn on time.

According to Fig. 4, the gate drive current I_{G_on} is

$$I_{G\_on} = I_{G\_off} = i_{Lr}(t_1) = \frac{V_c T_{pre}}{L_r} \tag{3}$$

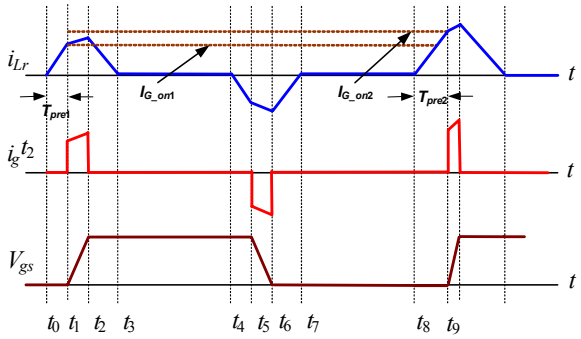


Fig. 4 Key waveforms of the discontinuous CSD

The control sequence of the four drive switches S_1-S_2-S_3-S_4, along with the CS inductor current i_{Lr}, gate drive current i_g and the gate-to-source voltage of the power MOSFET Q are illustrated in Fig. 5. The key waveforms to note are: 1) the CS inductor current i_{Lr} is discontinuous to minimize the conduction loss of the CSD; 2) the gate drive current i_g is nearly constant to reduce the turn on and off switching time significantly.

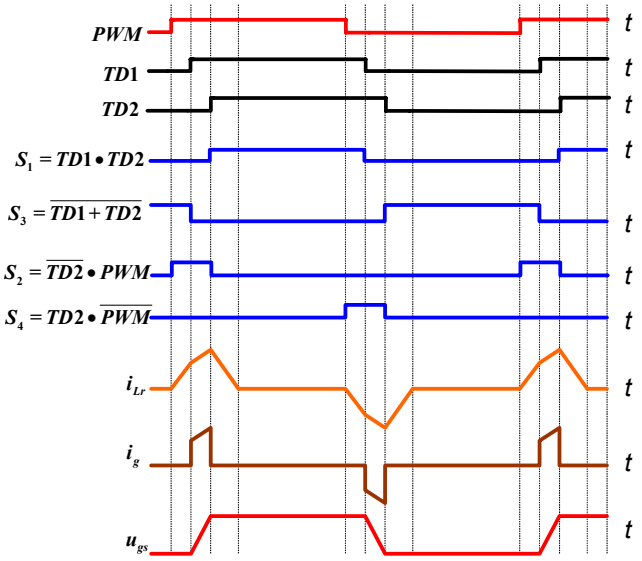


Fig. 5 The control sequence of the four drive switches S_1-S_4, the CS inductor current i_{Lr}, gate drive current i_g and gate-to-source voltage of the power MOSFET

The discontinuous CSD also can achieve adaptive drive current to switching current of the power MOSFET.

From (3) and Fig. 4, it is interesting to notice that the drive current of the discontinuous CSD is proportional to the pre-charge time, which is normally fixed when the control circuit is designed. So the idea is that if the pre-charge time can be varied according to different load, then adaptive drive current can be realized. As show in Fig. 4, if the load current increase, the switch current will increase accordingly, so the switching loss of the power MOSFET increase. We can increase the pre-charge time from T_{pre1} to T_{pre2}, so the gate drive current increased adaptively to reduce the switching loss.

III. Comparison and Optimization of Continuous and Discontinuous CSD for MHz PFC Applications

A. Drive circuit analysis

Both the continuous CSD and discontinuous CSD use the inductor as a current source. The energy stored in the inductance can be recovered to the driver supply voltage rail. The efficiency of gate energy recovery depends on the loss of the CSD circuit.

The drive loss includes: 1) the resistive loss caused by the impedance of the driver switches, P_{cond}, 2) the loss of the current source inductor L_r, P_{ind}; 3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs, P_{RG}; 4) gate drive loss of drive switches, P_{gate}.

Therefore, the total loss CSD is

$$P_{Drive} = P_{cond} + P_{ind} + P_{RG} + P_{gate} \quad (4)$$

Fig. 6 shows the drive loss comparison between the continuous and discontinuous at the switching frequency of 1 MHz. The components used are as follows: drive switches S_1-S_4: FDN335N; CS inductors: L_r=100nH (1812SMS) for the discontinuous, and L_r=1μH (DS3316P) for the continuous.

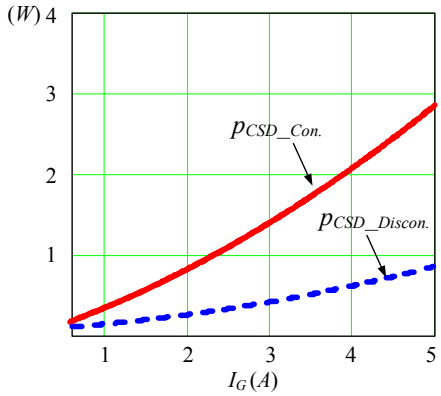


Fig. 6 Drive loss comparison between the continuous CSD and discontinuous CSD at 1MHz with different gate currents

It is observed that for the same gate drive current I_G, the discontinuous CSD has much lower drive loss than the continuous one, since the continuous current is a triangle waveform with larger RMS value and thus higher conduction loss.

B. Switching Loss Reduction and Adaptive Drive Current

Both of the continuous and discontinuous CSDs can achieve fast switching speed and reduce the switching losses significantly since they can use the inductor current as constant current source.

Normally, for the continuous CSD, the current inductor value is relatively high, which is typically around 1μH at the switching frequency of 1MHz. Furthermore , the peak value of the circulating current will changes with the duty cycle D, which changes with input line voltage. Fig. 3 gives the adaptive drive current in half line period.

For the discontinuous CSD, referring to Fig. 4, the peak value of the circulating current is determined by the pre-charge time, so the drive current can keep constant in half line period, if the load current is not changed.

In comparison, the discontinuous CSD has much lower inductor value, which is around 100nH at 1MHz switching frequency typically. This significant inductance reduction leads to the size shrink and board area reduction. More importantly, the inductance is independent of the switching frequency so that variable frequency control can be used with this type of CSDs.

Furthermore, the discontinuous CSD has discontinuous inductor current and thus low conduction losses. Compared to the continuous CSD solutions, the gate drive current of the discontinuous CSD can be chosen higher to further reduce the switching loss.

Fig. 7 shows the comparison of the 1MHz PFC loss distribution between the continuous CSD and conventional driver, and Fig. 8 shows the comparison between the discontinuous CSD and conventional driver. From Fig. 7 and Fig. 8, it can be seen that, due to the higher drive current, the

discontinuous CSD can achieve more switching loss reduction, so the total loss reduction can be achieved.

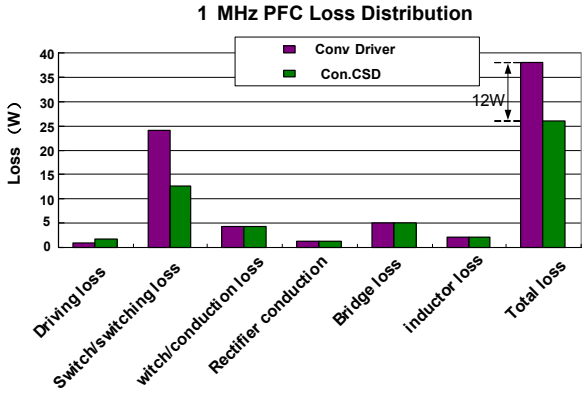


Fig. 7 Loss breakdown between the continuous CSD and the conventional driver at 1MHz (Vin=110Vac, Vo=380V, Vc=15V, Po=300W and Lr=1uH)

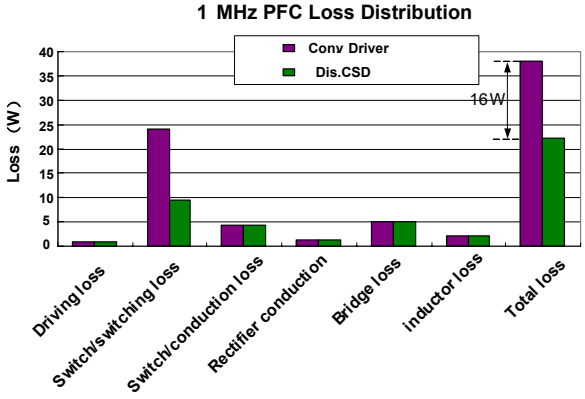


Fig. 8 Loss breakdown between the discontinuous CSD and the conventional driver at 1MHz (Vin=110Vac, Vo=380V, Vc=15V, Po=300W and Lr=100uH)

C. Interleaving Comparison for Continuous and Discontinuous

One advantage of the continuous CSD is that can be directly used to drive two interleaving boost PFC converters as shown in Fig. 9. Fig. 10 gives the key waveforms. The advantage is that only one continuous FB CSD is required and the ripple cancellation effect of the boost PFC converters is also achieved, while there will use two discontinuous FB CSD to drive the interleaving boost PFC converter.

Moreover, the commercial buck driver with two complimentary drive signals can be directly used to the continuous CSD circuit. This much reduce the complexity of the CSD circuit implementation with discrete components compared to the discontinuous CSD.

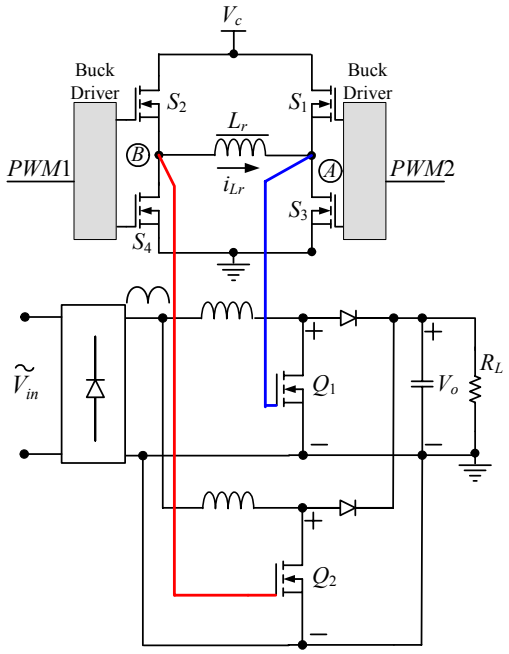


Fig. 9 Interleaving boost PFC converters with the continuous CSD

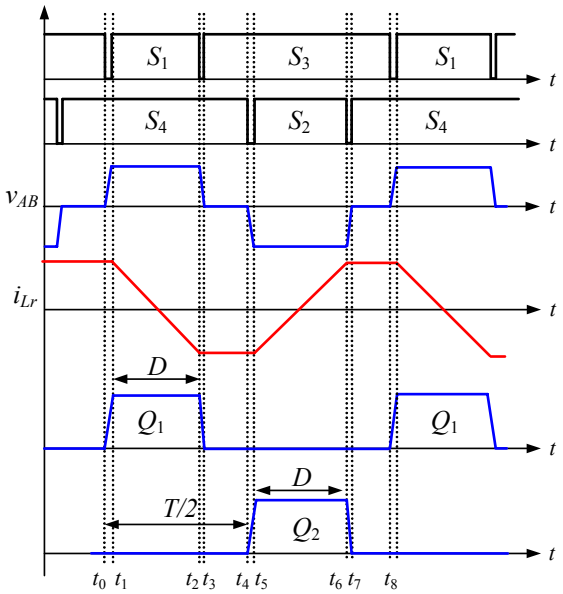


Fig. 10 Key waveforms of the interleaving boost PFC converters with continuous CSD

D. Adaptive Drive Current for MHz PFC Applications

Both the continuous and discontinuous CSDs can achieve adaptive drive current for MHz boost PFC applications.

With certain load, when the input line voltage is low, the continuous CSD solution for the boost PFC converters proposed can achieve adaptive drive current inherently in some range of the operation of the converter. From Fig. 11, from t_0 to t_1, it can be seen that the continuous CSD can achieve adaptive drive current to the input current. But,

essentially, the gate drive current of the continuous CSD is only adaptive to the duty cycle which varies with the input line voltage.

Fig. 11 shows that when during t_1 and t_2, the load current increases, the peak current of the boost inductor will also increase, the dotted line shows that the peak gate drive current of the continuous CSD keeps unchanged, which is not able to be adaptive to load current. This is the greatest weakness of the continuous CSD for MHz PFC applications.

In order to solve the shortcomings of the continuous CSD for MHz PFC applications, the discontinuous CSD with adaptive drive current is investigated for MHz switching frequency PFC. By sensing average of the boost inductor current, we can adjust the pre-charge time to change the gate drive current of the discontinuous CSD, so that the drive current can be adaptive to the load current. Fig. 11 shows that when the load current increases between t_1 and t_2, the pre-charge time increased to be adaptive to the load current, so the discontinuous CSD could provide high gate current to further reduce the switching loss, and the efficiency of the MHz PFC can be improved in a wide load range.

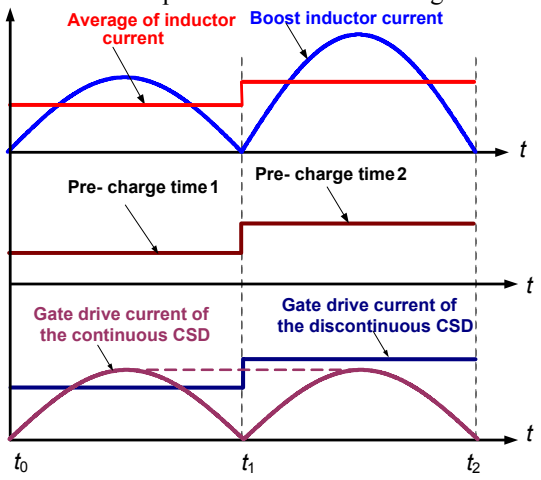


Fig. 11 The adaptive drive current with different loads

E. Optimal Design

For a given application, in order to achieve fast switching speed, the gate drive current should be chosen properly. The design tradeoff is between switching speed, which translates into reduced switching loss, and gate drive loss.

In order to find the optimized gate drive current, the objective function of the gate drive current I_{G_on} is established by adding the switching loss and the CSD circuit loss together as:

$$F(I_G) = P_{switching\_loss}(I_G) + P_{CSD}(I_G) \quad (5)$$

The object function is a U-shape curve as function of the drive current I_G, and the optimization solution is simply located at the lowest point of the curve.

Based on the same idea, Fig. 12 and Fig. 13 illustrate the optimal curve for the continuous and discontinuous CSD in MHz PFC applications, which includes the switching loss $p_{switching\ loss}$, the CSD circuit loss p_{CSD} and the objective function $F(I_G)$ as function of the gate drive current I_{gmax} and I_g. The specifications of the boost PFC converter are: V_{in}=110Vac; V_o=380V; P_o=200W; V_c=12V; f_s=1MHz; power MOSFET Q: SPA11N60C3; boost diode: CSD06060 and L_f=100uH.

It is observed that $F(I_G)$ is a U-shaped curve, and therefore, the optimization solution can be found at the lowest point of the curve. As we know, the drive current of the continuous CSD changes with the input line current adaptively in half line period, we choose the max drive current of the continuous CSD as the optimal value. For the continuous CSD, the max optimal drive current I_{Gmax} is chosen as 3.2A. For the discontinuous one, while the optimal drive current is 3.5A and is constant during the line period. This is because the continuous CSD has higher drive circulating loss over the discontinuous one as shown in Fig. 6, which limits the optimal drive current value. Fig. 14 gives the comparison of the drive current in half line period with 110Vac input line voltage. From Fig. 14, it can be seen that the continuous CSD can achieve adaptive drive current to the input line current in half line period, and the max optimal drive current is 3.2A. The optimal drive current of the discontinuous CSD is 3.5A and keeps constant in half line period. This means that the discontinuous CSD can achieve higher effective drive current during half line period and thus more switching loss reduction.

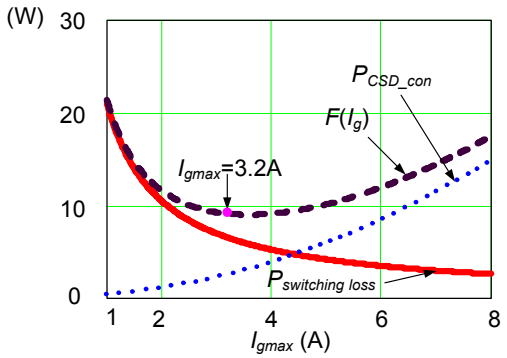


Fig. 12 Optimal function $F(I_G)$ as function of current I_{Gmax}: continuous

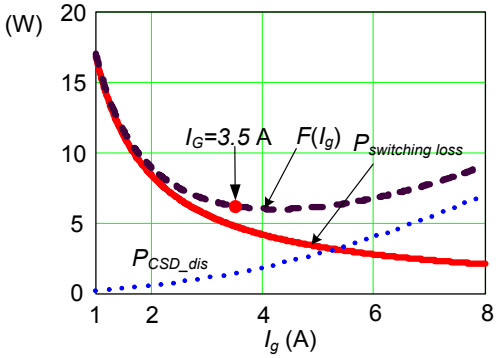


Fig. 13 Optimal function $F(I_G)$ as function of current I_G: discontinuous

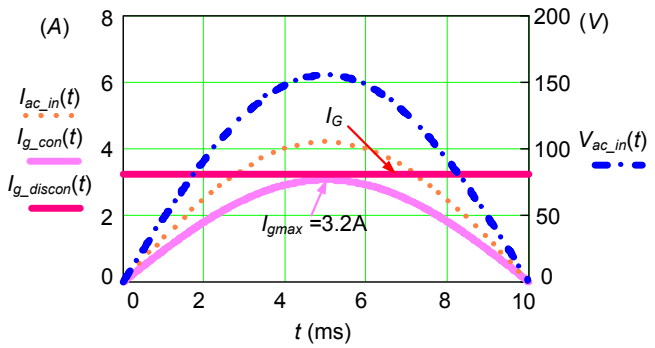


Fig. 14 The optimal drive current I_{gmax}: continuous and I_G: discontinuous in half line period

IV. Experimental Results and Discussion

The 380V/200W output and 1MHz boost PFC converters with continuous and discontinuous CSDs were built to verify the comparison of the two drive circuits. The CSDs are used for the power MOSFET. The gate driver voltage V_c=12V. The specifications are: boost inductor L=100μH; output capacitance C=220μF; power MOSFET: SPA11N60C3; the boost diode: CSD06060; the CS inductor of continuous CSD L_r=1μH (DS3316P); the CS inductor of discontinuous CSD L_r=100nH (1812SMS). It should be noted that no commercial PFC IC chip is available for 1 MHz switching frequency PFC application.

Fig. 15 shows the input line voltage and current of the boost PFC with continuous CSD, and Fig. 16 gives the discontinuous CSD. Both the continuous and discontinuous CSDs are suitable for boost PFC applications. The measured PF values are given in Table I according to different loads. It is observed that the PF values are all above 0.99, which are compatible to the industrial standards. The functionality of the power factor correction is realized with the continuous and discontinuous CSD.

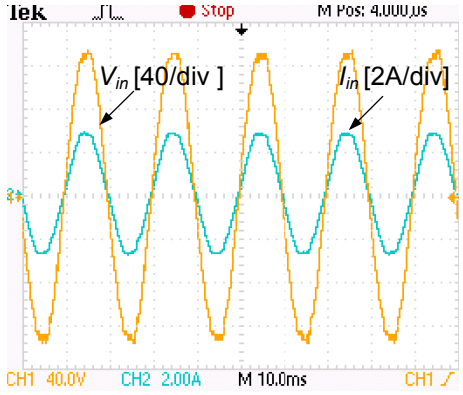


Fig. 15 The input line voltage and current of the boost PFC with continuous CSD

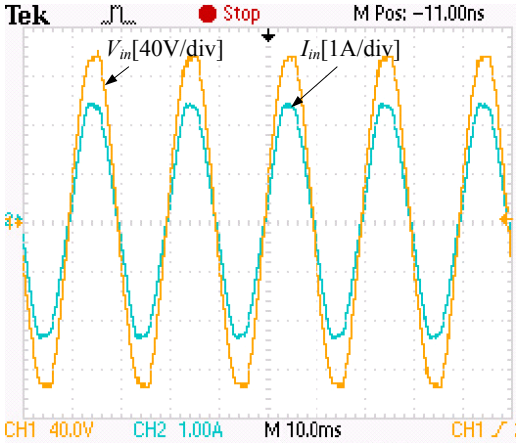


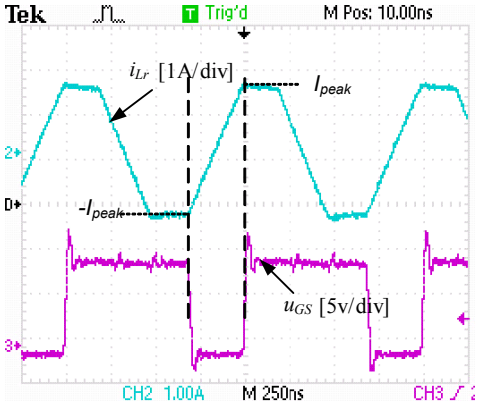
Fig. 16 The input line voltage and current of the boost PFC with discontinuous CSD

Table Ⅰ Measured PF values at different loads under 110VAC.

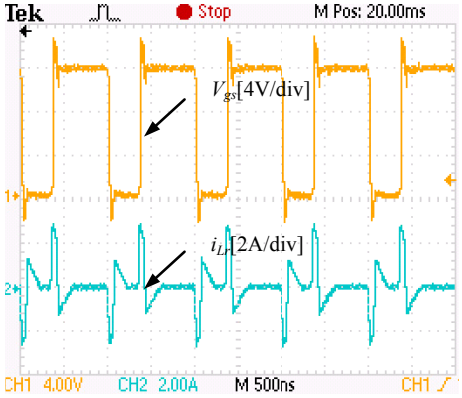
Load Conditions (W)	25% (50W)	50% (100W)	75% (150W)	100% (200W)
PF (continuous)	0.992	0.994	0.998	0.999
PF (discontinuous)	0.993	0.994	0.998	0.999

Fig. 17(a) shows the CS inductor current i_{Lr} and the gate drive signals u_{GS} with the continuous CSD. The inductor current is triangle waveform and agrees with the theory waveform in Fig. 2.

In comparison, Fig. 17(b) illustrates the waveforms of i_{Lr} and u_{GS} for discontinuous CSD. The inductor current is discontinuous as expected. During the pre-charge time, the inductor current ramps up. After the designed the pre-charge time, the inductor current continues to ramp up at a decreasing rate while at the same time charge the gate of the control MOSFET during the turn on interval.



(a) Continuous CSD



(b) Discontinuous CSD

Fig. 17 Gate signals v_{gs_Q1} and CS inductor current i_{Lr}

Fig. 18 shows that they both can achieve higher efficiency over the conventional voltage source driver (VSD) owing to higher gate driver and switching loss reduction. Compared to the continuous CSD, the discontinuous CSD has no circulating current, so the drive loss is lower, and the gate drive current can be designed with higher value. Fig. 18 shows that the discontinuous CSD achieves higher efficiency over the continuous CSD due to higher gate drive current.

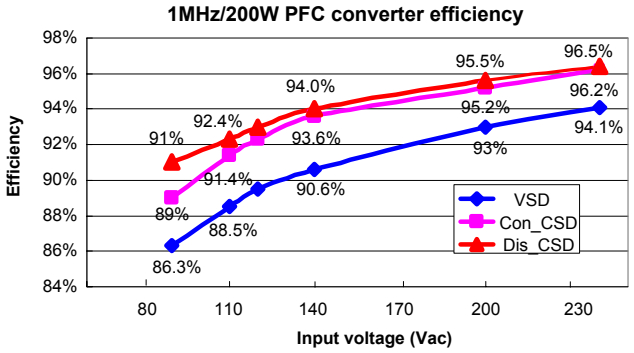


Fig. 18 Efficiency comparison at different input voltages

V. Conclusion

In this paper, comprehensive comparison of the continuous and discontinuous CSDs is presented in terms of switching loss reduction, gate energy recovery and adaptive solutions. Compared to the discontinuous CSD, one of the advantages of the continuous CSD is that can be directly used to drive two interleaving boost PFC converters, so the ripple cancellation effect of the boost PFC converters can be achieved. Compared to the continuous CSD, the discontinuous CSD can achieve high gate drive current and low drive circuit losses. This leads to higher efficiency of the discontinuous mode over the continuous mode in whole input voltage range and load condition. With 90Vac input, 380V/200W output, the discontinuous CSD achieves an efficiency improvement of 2% (from 89% to 91%) over the continuous CSD. They are all able to achieve boost PFC functionalities at high frequency.

Nevertheless, the discontinuous CSD needs more drive switches and complex control. Owing to the integrated circuit technology, this drawback can be solved when the CSDs are integrated as a drive chip. The experimental results verified the difference of the two types of the CSD circuits.

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